REMARKS

This paper is responsive to the Final Office Action dated April 29, 2004. Claims 1-32 were examined. Claims 1-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,591,383 to Michel et al. in view of U.S. Patent No. 6,623,183 to Peragine. Claims 1-14 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,835,501 to Dalmia et al. in view of Peragine. Claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dalmia in view of Peragine in further view of U.S. Patent No. 5,764,651 to Bullock et al. Claims 16-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Michel in view of Peragine, in further view of Dalmia. Claims 20-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dalmia in view of Peragine. Claims 24-30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dalmia in view of Peragine, in further view of U.S. Patent No. 5,305,323 to Lada. Claims 31 and 32 stand rejected under 35 U.S.C. § 103 as being unpatentable over Dalmia in view of Peragine, in further view of Bullock.

Claims 1-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Michel et al. in view of Peragine. Regarding claim 1, Applicant respectfully maintains that Michel, alone or in combination with Peragine, fails to teach or suggest

> generating a count value according to how many of the first time intervals have at least one transition that occurred in the predetermined phase zone, the count value corresponding to the bit error rate,

as recited in claim 1. Michel teaches detecting an error rate of a data stream by counting the number of bad blocks in a detection interval to a threshold value. Abstract. Michel also teaches at col. 5, lines 20-35, computing errors with a BIP2 calculation, "comprising a 2-bit result in which one bit is the XOR of all of the even bits in a given data frame, and the other bit is the XOR of all of the odd bits." Nowhere does Michel teach or suggest generating a count value according to how many of the first time intervals have at least one transition that occurred in the predetermined phase zone. Peragine fails to compensate for the shortcomings of Michel. Peragine teaches counting the number of transitions in a sampling window. (Col. 3, line 63-col.

4, line 10) However, Peragine fails to teach or suggest counting the number of first time intervals having at least one transition occurring in a predetermined phase zone, as required by claim 1. For at least this reason, Applicant respectfully maintains that claim 1 distinguishes over Michel and all references of record. Accordingly, Applicant respectfully requests that the rejection of claim 1, and all claims dependent thereon, be withdrawn.

Regarding claim 11, Applicant respectfully maintains that Michel, alone or in combination with Peragine, fails to teach or suggest

> generating a count according to how many of the first time intervals have at least one transition that occurred in the predetermined phase zone,

as recited in claim 11. Michel teaches detecting an error rate of a data stream by counting the number of bad blocks in a detection interval to a threshold value. Abstract. Michel also teaches at col. 5, lines 20-35, computing errors with a BIP2 calculation, "comprising a 2-bit result in which one bit is the XOR of all of the even bits in a given data frame, and the other bit is the XOR of all of the odd bits." Nowhere does Michel teach or suggest generating a count value according to how many of the first time intervals have at least one transition that occurred in the predetermined phase zone. Peragine fails to compensate for the shortcomings of Michel. Peragine teaches counting the number of transitions in a sampling window. (Col. 3, line 63-col. 4, line 10) However, Peragine fails to teach or suggest counting the number of first time intervals having at least one transition occurring in a predetermined phase zone, as required by claim 11. For at least this reason, Applicant respectfully maintains that claim 11 distinguishes over Michel and all references of record. Accordingly, Applicant respectfully requests that the rejection of claim 11, and all claims dependent thereon, be withdrawn.

Regarding claim 13, Applicant respectfully maintains that Michel, alone or in combination with Peragine, fails to teach or suggest

> means for determining a bit error rate according to how many of a plurality of evaluation intervals have one or more transitions in the predefined phase zone,

as recited in claim 13. Michel teaches detecting an error rate of a data stream by counting the number of bad blocks in a detection interval to a threshold value. Abstract. Michel also teaches at col. 5, lines 20-35, computing errors with a BIP2 calculation, "comprising a 2-bit result in which one bit is the XOR of all of the even bits in a given data frame, and the other bit is the XOR of all of the odd bits." Nowhere does Michel teach or suggest determining a bit error rate according to how many of a plurality of evaluation intervals have at least one transition that occurred in a predefined phase zone. Peragine fails to compensate for the shortcomings of Michel. Peragine teaches counting the number of transitions in a sampling window. (Col. 3, line 63-col. 4, line 10) However, Peragine fails to teach or suggest determining a bit error rate according to how many of a plurality of evaluation intervals have at least one transition that occurred in a predefined phase zone, as required by claim 13. For at least this reason, Applicant respectfully maintains that claim 13 distinguishes over Michel and all references of record. Accordingly, Applicant respectfully requests that the rejection of claim 13, and all claims dependent thereon, be withdrawn.

Regarding claim 15, Applicant respectfully maintains that Michel, alone or in combination with Peragine, fails to teach or suggest

> determining a bit error rate according to how many of a plurality of evaluation intervals have one or more transitions in the predetermined portion of the sample clock period,

as recited in claim 15. Michel teaches detecting an error rate of a data stream by counting the number of bad blocks in a detection interval to a threshold value. Abstract. Michel also teaches at col. 5, lines 20-35, computing errors with a BIP2 calculation, "comprising a 2-bit result in which one bit is the XOR of all of the even bits in a given data frame, and the other bit is the XOR of all of the odd bits." Nowhere does Michel teach or suggest determining a bit error rate according to how many evaluation intervals have at least one transition that occurred in the predetermined portion of a sample clock period. Peragine fails to compensate for the shortcomings of Michel. Peragine teaches counting the number of transitions in a sampling window. (Col. 3, line 63-col. 4, line 10) However, Peragine fails to teach or suggest determining

a bit error rate according to how many evaluation intervals have at least one transition that occurred in the predetermined portion of a sample clock period, as required by claim 15. For at least this reason, Applicant respectfully maintains that claim 15 distinguishes over Michel and all references of record. Accordingly, Applicant respectfully requests that the rejection of claim 15, and all claims dependent thereon, be withdrawn.

Claims 1-14 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,835,501 to Dalmia et al. in view of Peragine. Regarding claim 1, Applicant respectfully maintains that Dalmia, alone or in combination with Peragine, fails to teach or suggest

> generating a count value according to how many of the first time intervals have at least one transition that occurred in the predetermined phase zone, the count value corresponding to the bit error rate,

as recited in claim 1. Dalmia teaches varying the frequency or phase of a clock signal at a predetermined rate and determining the number of bit errors arising in a clock and data recovery unit. Dalmia teaches at col. 3, lines 32-40 a bit error test including "generating a jittered clock, using the jittered clock to generate a test data stream, feeding the test data stream to the CRU that is under test, and determining by the BER tester 3 the number of bit errors that arise in the CRUs recovered data stream." Dalmia fails to teach or suggest a phase zone of a sample clock or generating a count value according to how many of the first time intervals have at least one transition that occurred in the predetermined phase zone, the count value corresponding to the bit error rate.

The Office Action states that "Dalmia et al. does not explicitly point out to the first time intervals and does not limit the time of intervals, inherently suggesting the possibility to use any intervals including the first time interval." While a teaching may be express or inherent, inherency is a stringent standard.

> To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 U.S.P.Q.2D (BNA) 1746, 1749 (Fed. Cir. 1991). "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of

> circumstances is not sufficient." Id. at 1269, 20 U.S.P.Q.2D (BNA) at 1749 (quoting *In re Oelrich*, 666 F.2d 578, 581, 212 U.S.P.Q. 323, 326 (C.C.P.A. 1981).

See *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999); MPEP § 2112. Applicant disagrees that it is inherent for the system of Dalmia to practice the claim. For example, there is no teaching or suggestion that Dalmia must (or does) generate a count value according to how many of the first time intervals have at least one transition that occurred in the predetermined phase zone. To be inherent in generating a count value according to how many of the first time intervals have at least one transition that occurred in the predetermined phase zone, those functions must by necessity be performed in Dalmia. They are not.

In addition, the Office Action relies on Peragine to teach the first time intervals. Peragine teaches counting the number of transitions in a sampling window. (Col. 3, line 63-col. 4, line 10) However, Peragine fails to teach or suggest counting the number of first time intervals having at least one transition occurring in a predetermined phase zone, as required by claim 1. In addition, the Office Action states that "one of ordinary skill in the art would use well known principles of the predetermined phase zone (divided zone) in order to provide definition of the bit error rate." Applicant respectfully requests that the Examiner provide references in support of this position and explain how these references can be properly combined with other references of record to teach Applicant's claimed count value revealed in claim 1. Applicant respectfully maintains that claim 1 distinguishes over Dalmia and all references of record. Accordingly, Applicant respectfully requests that the rejection of claim 1, and all claims dependent thereon, be withdrawn.

Regarding claim 11, Applicant respectfully maintains that Dalmia, alone or in combination with Peragine, fails to teach or suggest

> generating a count according to how many of the first time intervals have at least one transition that occurred in the predetermined phase zone,

as recited in claim 11. Dalmia teaches varying the frequency or phase of a clock signal at a predetermined rate and determining the number of bit errors arising in a clock and data recovery

unit. Dalmia teaches at col. 3, lines 32-40 a bit error test including "generating a jittered clock, using the jittered clock to generate a test data stream, feeding the test data stream to the CRU that is under test, and determining by the BER tester 3 the number of bit errors that arise in the CRUs recovered data stream." Dalmia fails to teach or suggest generating a count according to how many of the first time intervals have at least one transition that occurred in the predetermined phase zone.

The Office Action states that "Dalmia et al. does not explicitly point out to the first time intervals and does not limit the time of intervals, inherently suggesting the possibility to use any intervals including the first time interval." While a teaching may be express or inherent, inherency is a stringent standard. See *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999); MPEP § 2112. Applicant disagrees that it is inherent for the system of Dalmia to practice the claim. For example, there is no teaching or suggestion that Dalmia must (or does) generate a count according to how many of the first time intervals have at least one transition that occurred in the predetermined phase zone. To be inherent in generating a count value according to how many of the first time intervals have at least one transition that occurred in the predetermined phase zone, those functions must by necessity be performed in Dalmia. They are not.

In addition, the Office Action relies on Peragine to teach the first time intervals. Peragine teaches counting the number of transitions in a sampling window. (Col. 3, line 63-col. 4, line 10) However, Peragine fails to teach or suggest counting the number of first time intervals having at least one transition occurring in a predetermined phase zone, as required by claim 11. In addition, the Office Action states that "one of ordinary skill in the art would use well known principles of the predetermined phase zone (divided zone) in order to provide definition of the bit error rate." Applicant respectfully requests that the Examiner provide references in support of this position and explain how these references can be properly combined with other references of record to teach Applicant's claimed count according to how many of the first time intervals have at least one transition that occurred in the predetermined phase zone revealed in claim 11. Applicant respectfully maintains that claim 11 distinguishes over Dalmia and all references of record. Accordingly, Applicant respectfully requests that the rejection of claim 11, and all claims dependent thereon, be withdrawn.

Regarding claim 13, Applicant respectfully maintains that Dalmia, alone or in combination with Peragine, fails to teach or suggest

> means for determining a bit error rate according to how many of a plurality of evaluation intervals have one or more transitions in the predefined phase zone,

as recited in claim 13. Dalmia teaches varying the frequency or phase of a clock signal at a predetermined rate and determining the number of bit errors arising in a clock and data recovery unit. Dalmia teaches at col. 3, lines 32-40 a bit error test including "generating a jittered clock, using the jittered clock to generate a test data stream, feeding the test data stream to the CRU that is under test, and determining by the BER tester 3 the number of bit errors that arise in the CRUs recovered data stream." Dalmia fails to teach or suggest determining a bit error rate according to how many of a plurality of evaluation intervals have one or more transitions in the predefined phase zone.

The Office Action states that "Dalmia et al. does not explicitly point out to the first time intervals and does not limit the time of intervals, inherently suggesting the possibility to use any intervals including the first time interval." While a teaching may be express or inherent, inherency is a stringent standard. See *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999); MPEP § 2112. Applicant disagrees that it is inherent for the system of Dalmia to practice the claim. For example, there is no teaching or suggestion that Dalmia must (or does) determine a bit error rate according to how many of a plurality of evaluation intervals have one or more transitions in the predefined phase zone. To be inherent in determining a bit error rate according to how many of a plurality of evaluation intervals have one or more transitions in the predefined phase zone, those functions must by necessity be performed in Dalmia. They are not.

In addition, the Office Action relies on Peragine to teach the evaluation intervals. Peragine teaches counting the number of transitions in a sampling window. (Col. 3, line 63-col. 4, line 10) However, Peragine fails to teach or suggest determining how many of a plurality of evaluation intervals having at least one transition in a predetermined phase zone, as required by claim 13. In addition, the Office Action states that "one of ordinary skill in the art would use well known principles of the predetermined phase zone (divided zone) in order to provide

definition of the bit error rate." Applicant respectfully requests that the Examiner provide references in support of this position and explain how these references can be properly combined with other references of record to teach Applicant's claimed determination of a bit error rate according to how many of a plurality of evaluation intervals have one or more transitions in the predefined phase zone revealed in claim 13. Applicant respectfully maintains that claim 13 distinguishes over Dalmia and all references of record. Accordingly, Applicant respectfully requests that the rejection of claim 13, and all claims dependent thereon, be withdrawn.

Claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dalmia in view of Peragine in further view of U.S. Patent No. 5,764,651 to Bullock et al. Applicant respectfully maintains that Dalmia, alone or in combination with Peragine, fails to teach or suggest

> determining a bit error rate according to how many of a plurality of evaluation intervals have one or more transitions in the predetermined portion of the sample clock period,

as recited in claim 15. Dalmia teaches varying the frequency or phase of a clock signal at a predetermined rate and determining the number of bit errors arising in a clock and data recovery unit. Dalmia teaches at col. 3, lines 32-40 a bit error test including "generating a jittered clock, using the jittered clock to generate a test data stream, feeding the test data stream to the CRU that is under test, and determining by the BER tester 3 the number of bit errors that arise in the CRUs recovered data stream." Dalmia fails to teach or suggest determining a bit error rate according to how many of a plurality of evaluation intervals have one or more transitions in the predetermined portion of the sample clock period.

Peragine and Bullock fail to compensate for the shortcomings of Dalmia. Peragine teaches counting the number of transitions in a sampling window. (Col. 3, line 63-col. 4, line 10) However, Peragine fails to teach or suggest determining a bit error rate according to how many of a plurality of evaluation intervals have one or more transitions in the predetermined portion of the sample clock period, as required by claim 15. Bullock teaches comparing bit interleave parity of a frame compared with a calculated value for the frame. (Col. 6, lines 59-64)

However, Bullock fails to teach or suggest determining a bit error rate according to how many of a plurality of evaluation intervals have one or more transitions in the predetermined portion of the sample clock period.

For at least these reasons, Applicant respectfully maintains that claim 15 distinguishes over Dalmia and all references of record. Accordingly, Applicant respectfully requests that the rejection of claim 15, and all claims dependent thereon, be withdrawn.

Claims 20-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dalmia in view of Peragine. Regarding claim 20, Applicant respectfully maintains that Dalmia, alone or in combination with Peragine, fails to teach or suggest

> determining how many of a plurality of evaluation intervals have one or more transitions in the predetermined portion of the sample clock period and supplying an indication thereof,

as recited in claim 20. Dalmia teaches varying the frequency or phase of a clock signal at a predetermined rate and determining the number of bit errors arising in a clock and data recovery unit. Dalmia teaches at col. 3, lines 32-40 a bit error test including "generating a jittered clock, using the jittered clock to generate a test data stream, feeding the test data stream to the CRU that is under test, and determining by the BER tester 3 the number of bit errors that arise in the CRUs recovered data stream." Dalmia fails to teach or suggest how many of a plurality of evaluation intervals have one or more transitions in the predetermined portion of the sample clock. Peragine fails to compensate for the shortcomings of Dalmia. Peragine teaches counting the number of transitions in a sampling window. (Col. 3, line 63-col. 4, line 10) However, Peragine fails to teach or suggest determining how many of a plurality of evaluation intervals have one or more transitions in the predetermined portion of the sample clock, as required by claim 20.

In addition, Dalmia, alone or in combination with Peragine fails to teach or suggest

> monitoring the indication to determine satisfactory performance of the integrated circuit,

as recited in claim 20. The Office Action states that "Dalmia et al. does not limit the monitoring the indication, inherently suggesting the possibility to use any monitoring including monitoring the indication to determine satisfactory." While a teaching may be express or inherent, inherency is a stringent standard. See *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999); MPEP § 2112. Applicant disagrees that it is inherent for the system of Dalmia to practice the claim. For example, there is no teaching or suggestion that Dalmia must (or does) monitor the indication of a plurality of evaluation intervals having one or more transitions in the predetermined portion of the sample clock period to determine satisfactory performance of the integrated circuit. To be inherent in monitoring the indication of a plurality of evaluation intervals having one or more transitions in the predetermined portion of the sample clock period to determine satisfactory performance of the integrated circuit, those functions must by necessity be performed in Dalmia. They are not. Peragine fails to compensate for the shortcomings of Dalmia. Since Peragine fails to teach or suggest supplying an indication of how many of a plurality of evaluation intervals have one or more transitions in the predetermined portion of the sample clock period, as discussed above, Peragine also fails to teach or suggest monitoring an indication of how many of a plurality of evaluation intervals have one or more transitions in the predetermined portion of the sample clock period to determine satisfactory performance of the integrated circuit.

For at least these reasons, Applicant respectfully maintains that claim 20 distinguishes over Dalmia, alone or in combination with other references of record. Accordingly, Applicant respectfully requests that the rejection of claim 20, and all claims dependent thereon, be withdrawn.

Regarding claim 23, Applicant maintains that Dalmia, alone or in combination with other references of record, fails to teach or suggest

> a bit error detect circuit coupled to determine if a bit error occurs in the input data stream according to whether an input data stream transition occurs in a predetermined phase zone of a sample clock used in the bit error detect circuit,

as recited by claim 23. Dalmia teaches varying the frequency or phase of a clock signal at a predetermined rate and determining the number of bit errors arising in a clock and data recovery unit. Dalmia teaches at col. 3, lines 32-40 a bit error test including "generating a jittered clock, using the jittered clock to generate a test data stream, feeding the test data stream to the CRU that is under test, and determining by the BER tester 3 the number of bit errors that arise in the CRUs recovered data stream." Dalmia fails to teach or suggest a phase zone of a sample clock or determining whether transitions of the input data stream occur in a predetermined portion of the sample clock. Peragine fails to compensate for the shortcomings of Dalmia. Peragine teaches counting the number of transitions in a sampling window. (Col. 3, line 63-col. 4, line 10) However, Peragine fails to teach or suggest determining whether transitions of the input data stream occur in a predetermined portion of the sample clock, as required by claim 23.

The Office Action states that "one of ordinary skill in the art would use well known principles of the predetermined phase zone (divided zone) in order to provide definition of the bit error rate." Applicant respectfully requests that the Examiner provide references in support of this position and explain how these references can be properly combined with other references of record to teach Applicant's claimed determination of whether transitions of the input data stream in a predetermined phase zone of a sample clock revealed in claim 23. Applicant respectfully maintains that claim 23 distinguishes over Dalmia, alone or in combination with other references of record. Accordingly, Applicant respectfully requests that the rejection of claim 23, and all claims dependent thereon, be withdrawn.

Claims 31 and 32 stand rejected under 35 U.S.C. § 103 as being unpatentable over Dalmia in view of Peragine, in further view of Bullock. Applicant respectfully maintains that Dalmia, alone or in combination with other references of record, fails to teach or suggest

> a counter circuit coupled to the phase zone detect circuit to supply a count indication of how many of a predetermined number of evaluation intervals have at least one transition that occurs in the predetermined phase zone of a sample clock,

as recited in claim 31. Dalmia teaches at col. 3, lines 32-40 a bit error test including "generating a jittered clock, using the jittered clock to generate a test data stream, feeding the test data stream to the CRU that is under test, and determining by the BER tester 3 the number of bit errors that arise in the CRUs recovered data stream." Dalmia fails to teach or suggest a predetermined phase zone of a sample clock or counting how many of a predetermined number of evaluation intervals have at least one transition that occurs in a predetermined phase zone of the sample clock. The Office Action admits that "Dalmia et al. does not explicitly point out to the 'sample clock'". Bullock teaches comparing bit interleave parity of a frame compared with a calculated value for the frame. (Col. 6, lines 59-64) However, Bullock fails to teach or suggest counting how many of a predetermined number of evaluation intervals have at least one transition that occurs in a predetermined phase zone of the sample clock.

Peragine fails to compensate for the shortcomings of Dalmia and Bullock. Peragine teaches counting the number of transitions in a sampling window. (Col. 3, line 63-col. 4, line 10) However, Peragine fails to teach or suggest supplying a count indication of how many of a predetermined number of evaluation intervals have at least one transition that occurs in a predetermined phase zone of the sample clock, as required by claim 23.

For at least this reason, Applicant respectfully maintains that claim 31 distinguishes over Dalmia, alone or in combination with other references of record. Accordingly, Applicant respectfully requests that the rejection of claim 31, and all claims dependent thereon, be withdrawn.

In summary, claims 1-32 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that, on the date shown below, this correspondence is being

☐ deposited with the US Postal Service with sufficient postage as first class mail, in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

☒ facsimile transmitted to the US Patent and Trademark Office.

Nicole Teitler Cave 6/29/04
Nicole Teitler Cave Date

EXPRESS MAIL LABEL: _____

Respectfully submitted,

Nicole Teitler Cave, Reg. No. 54,021
Attorney for Applicant(s)
(512) 338-6315
(512) 338-6301 (fax)